

MAYO FOUNDATION CHIP-TO-CHIP OPTICAL INTERCONNECT (C2OI) INITIATIVE

**Mayo Foundation
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Phone: 507-284-4056
June 23, 2003**

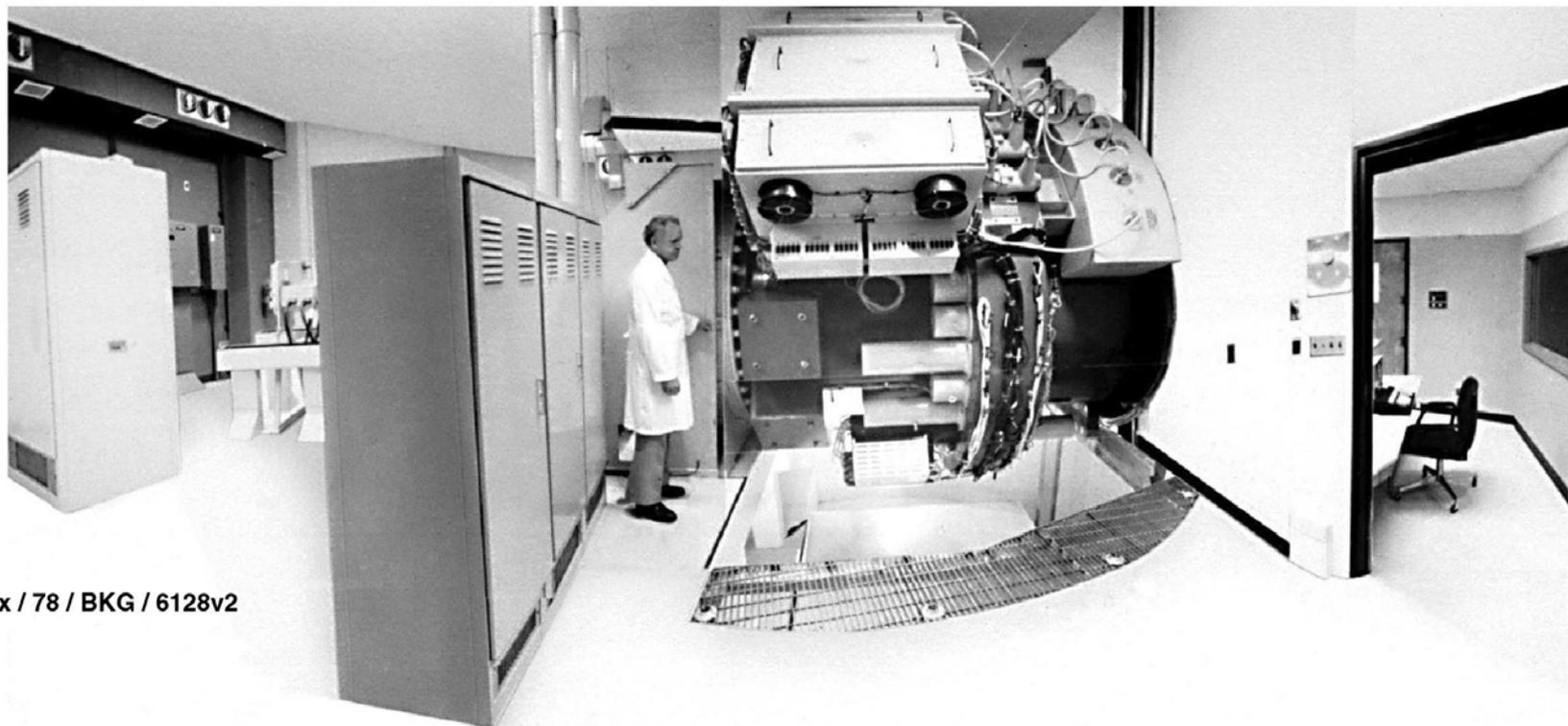
MAYO FOUNDATION OVERVIEW

- Charitable, not-for-profit organization
- Our mission is to provide the best medical care through integrated clinical practice, education, and research
- Mayo Foundation:
 - 45,536 total personnel, 2,808 physicians and scientists
 - \$3.4 billion in patient care revenue
- Mayo Foundation research team:
 - 2,288 total personnel
 - \$296.3 million in research funding, \$102.0 million in National Institute of Health funding
 - \$22.2 million in other federal funding
 - \$11.4 million to Special Purpose Processor Development Group (SPPDG)

MAYO SPPDG OVERVIEW

- Formed by Barry Gilbert in 1970 within the laboratory of Dr. Earl Wood
- Initial Mission: Develop special purpose high speed computers to create X-ray computed tomography images from raw data generated by Dynamic Spatial Reconstructor (DSR) funded by NIH
- Converted to DOD funding sources in 1978
- Our *primary* task: To develop advanced computer hardware & communications technology for the “DOD” and Intelligence Community
- Our *secondary* task: To transfer computer & secure communications technology to Mayo and to individual investigators within the Mayo Foundation
- Presently 53 FTEs (62 personnel) conducting 39 active research projects
- Not-for-profit organization, not engaged in competitive activities with any other program participants

**PHOTOGRAPH OF EXPERIMENTAL DYNAMIC SPATIAL RECONSTRUCTOR
THREE DIMENSIONAL X-RAY COMPUTED TOMOGRAPHY IMAGING MACHINE
(Side View of Rotating Gantry, Showing 14 X-ray Tubes and
14 Video Image Chains Mounted on Gantry; Designed in 1975;
Fabricated at Raytheon, Sudbury, MA; Installed at Mayo in 1978)**

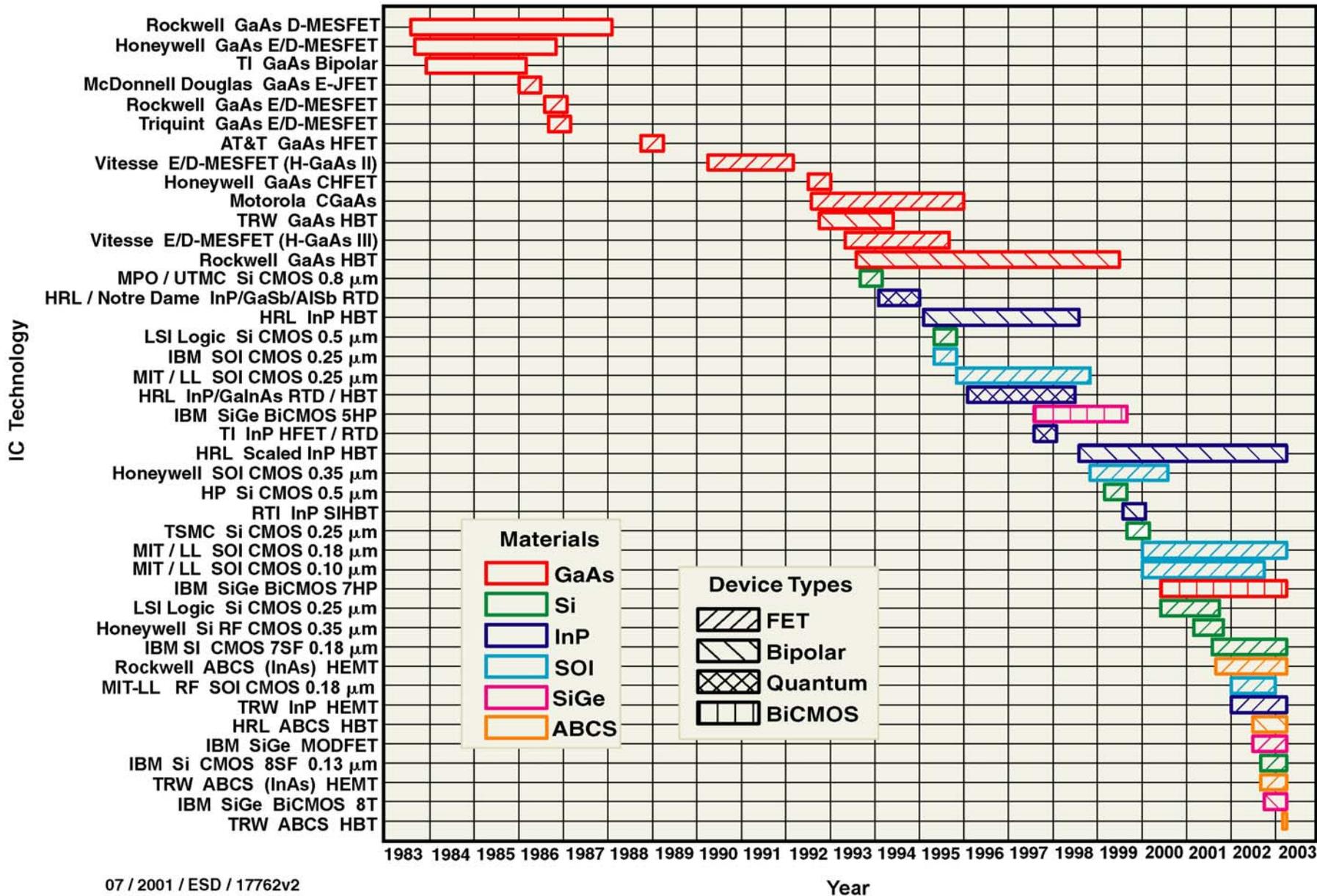


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SPPDG CORE COMPETENCIES

- **Specialized High Performance Integrated Circuit (IC) design and characterization:**
 - Silicon Germanium (SiGe)
 - Silicon on Insulator (SOI)
 - Indium Phosphide (InP)
 - Gallium Nitride (GaN)
 - Antimonide (Sb)
 - High Density CMOS
- Special purpose computer/system development
- Analog and microwave design and characterization
- Network and encryption systems for Government and Mayo
- Specialized applications for Micro-miniaturization of electronic systems and Micro Electro Mechanical Systems (MEMS)
- Photonic and Electronic Communication Systems Design and Prototypes
- On-chip and system level Signal Integrity (SI)
- Cleanroom based assembly, high speed digital bit error rate test (BERT) to 20 Gbps, and Microwave Vector Network Analysis capabilities to 220 GHz
- Anechoic chamber to 40 GHz

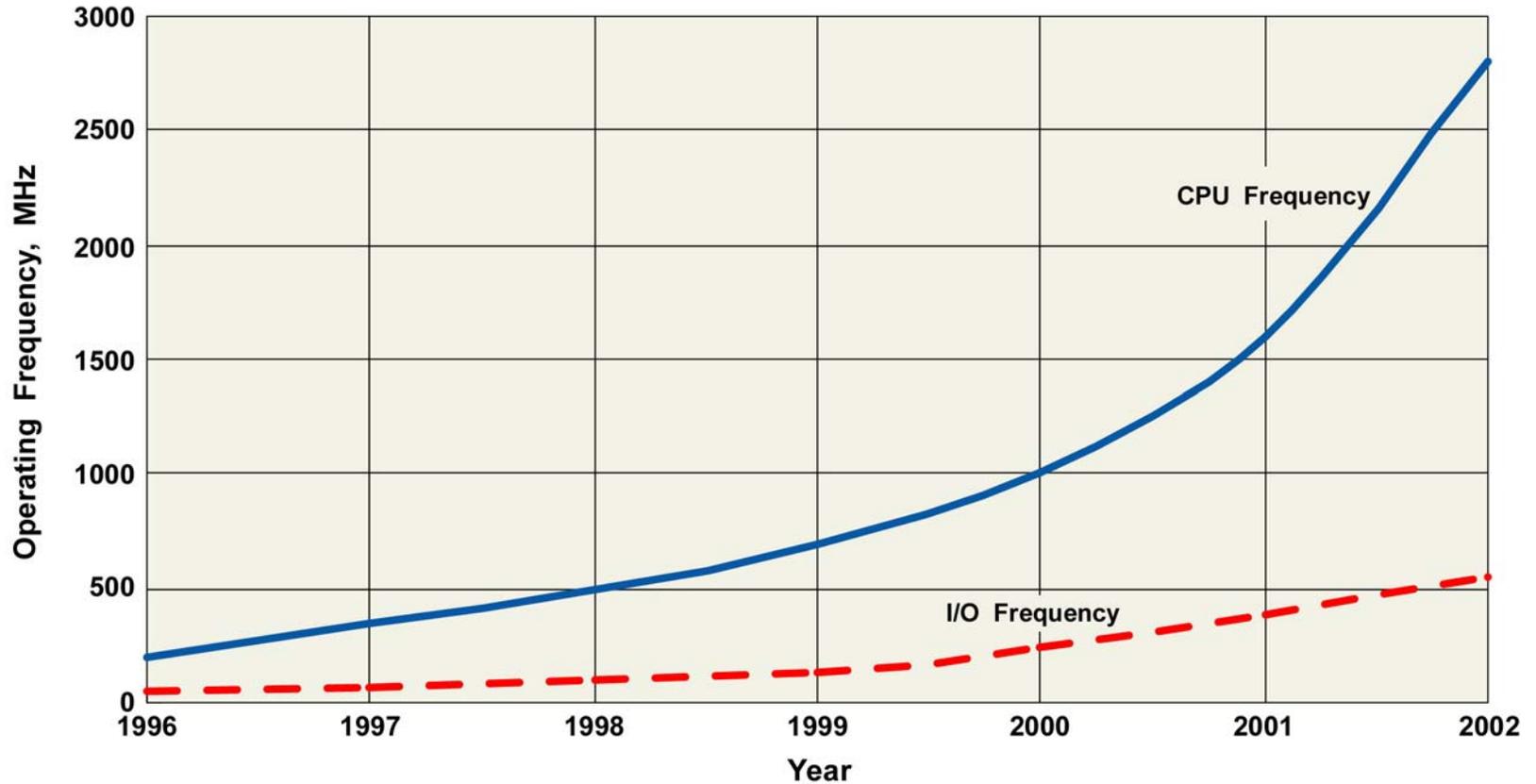
MAYO SPPDG IC TECHNOLOGY TIMELINE (March 31, 2003)



SYSTEM NEEDS FOR C2OI

- High End Compute Systems-Freightliner Parallel Processor
- Phased Array Antennas-Active Electronically Scanned Arrays (AESAs)
- Other?

A COMPARISON OF RECENT PROCESSOR CORE vs. EXTERNAL I/O OPERATING FREQUENCIES FOR PERSONAL COMPUTER SYSTEMS



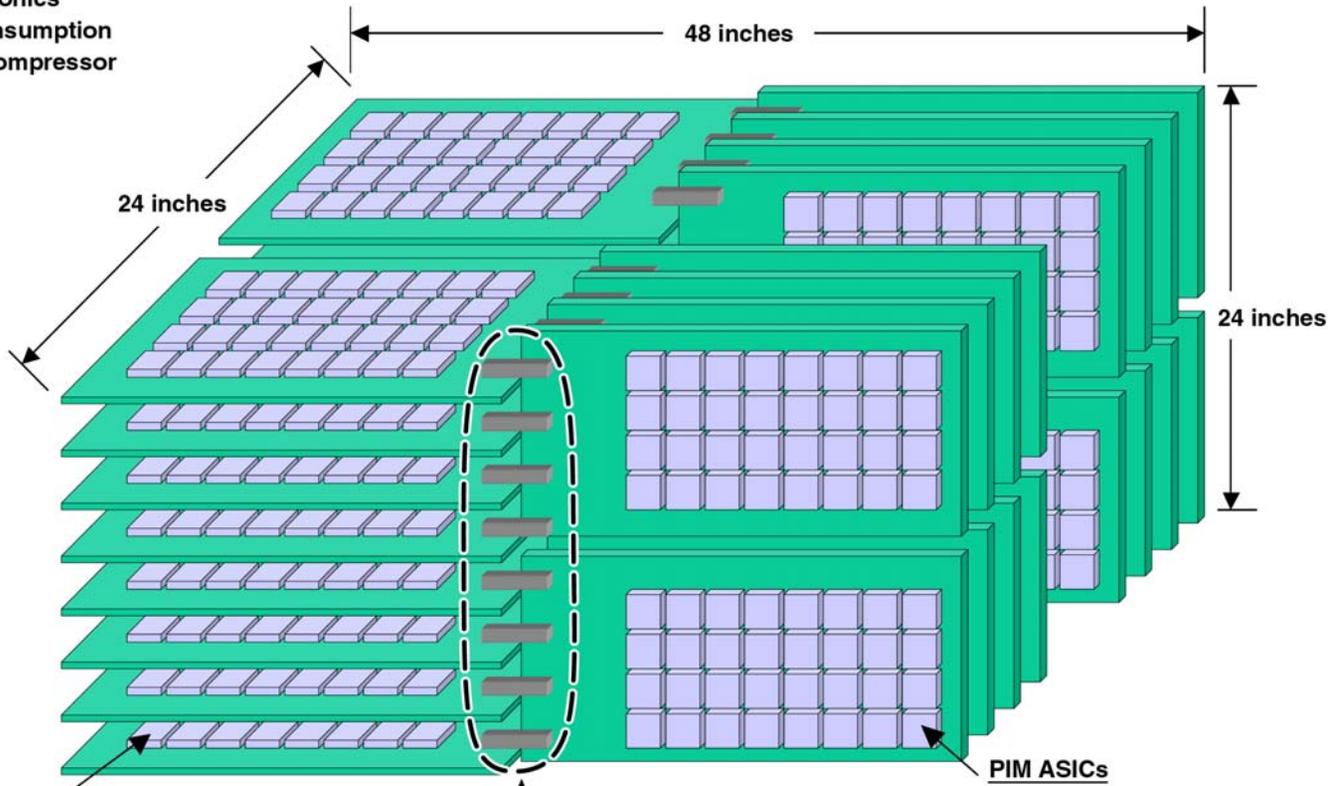
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BLOCK DIAGRAM OF CURRENT PARALLEL PROCESSOR SYSTEM DESIGN

System Overview

16 cubic foot of electronics
 68,000 watt power consumption
 Air cooled w/ 30 ton compressor
 27,000 amps at 2.5 V
 128 PIM boards
 8 peripheral boards
 ~4000 ASICs



Processor-in-Memory (PIM) Board

12.08 by 23.55 by 0.11 inch
 500 watt power consumption
 64 vertical, 64 horizontal PIM boards
 32 PIM ASICs per board

ORTHOGONAL CONNECTOR

CURRENT

64 single ended signals
 100 Mbps
 $64 \times 32 \times 32 \times 100 \text{ Mbps} = 6.6 \text{ Tbps}$
 BiSectional System
 Bandwidth (BSSBW)
 Satisfactory electrical distance

NEXT GENERATION

32 differential pair signals
 $32 \times 32 \times 32 \times 2.5 \text{ Gbps} = 82 \text{ Tbps BSSBW}$
 Electrical path distance limited:
 - Intra-Board < 5"
 - Inter-Board < 40"

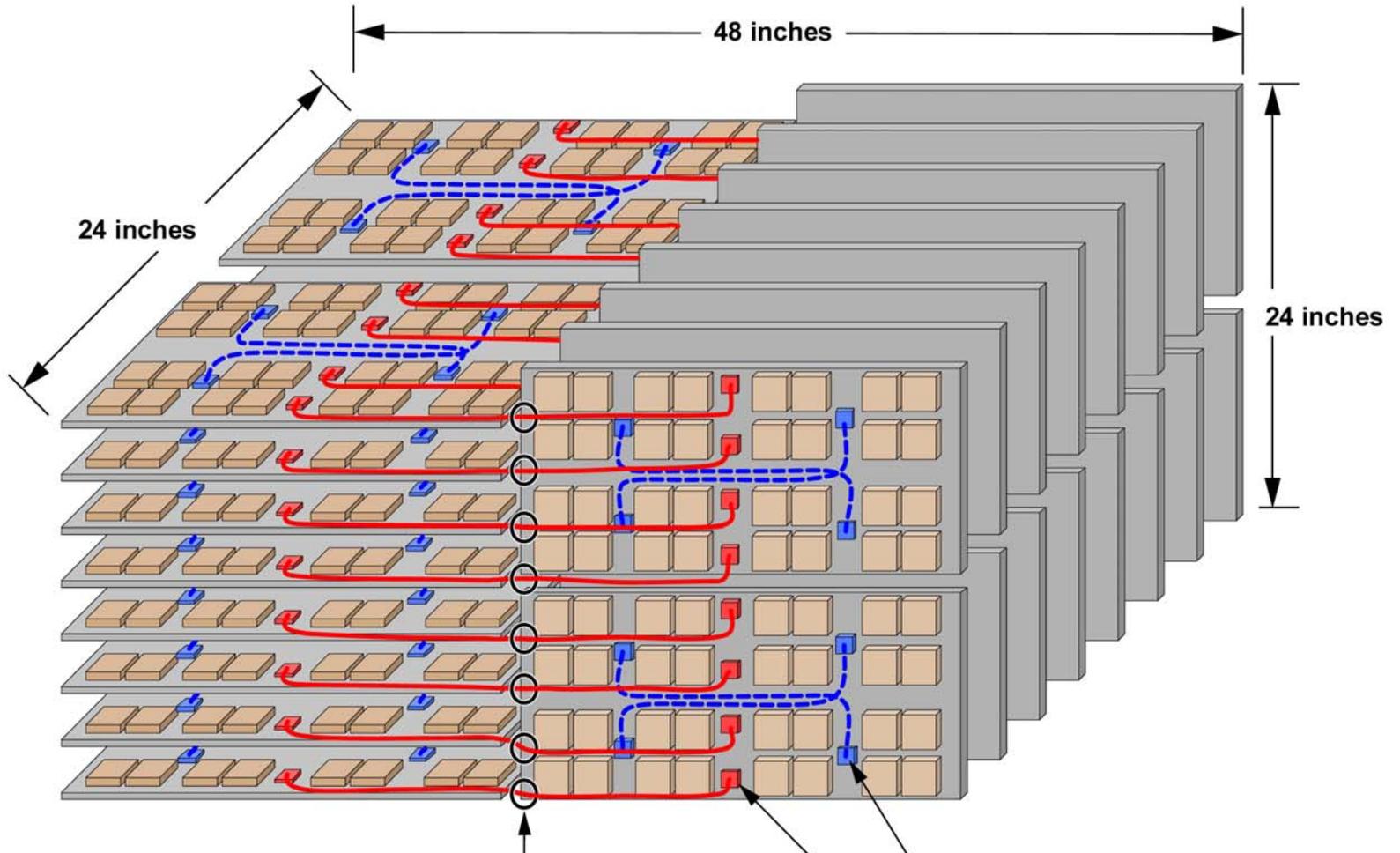
PIM ASICs
 0.25 mm CMOS from IBM
 50,000,000 devices, 15 watts @ 2.5 V
 16 by 16 by 0.4 mm silicon
 600-contact ball grid array package



C2OI PROGRAM OBJECTIVE

- Identify a system application where the C2OI program development objectives can make a significant impact on overall system performance
 - Example: High End Parallel Processor-Freightliner
 - Current max electrical bandwidth achieved: 6.6 Tbps Now
 - 64 single ended signals at 100 Mbps/ASIC
 - 32 ASICs/Motherboard
 - 32 Motherboards Stacked and Orthogonally Connected
 - Near term electrical system bw objective: 82 Tbps '04
 - 32 differential signals at 2.5 Gbps/ASIC
 - 32 ASICs/Motherboard
 - 32 Motherboards Stacked and Orthogonally Connected
 - Near term achievable C2OI program: 164-246 Tbps '04-'05
 - Additional advantages:
 - Effective “reach” distance improvement of 4-10x enables larger scale system designs
 - Potential hot plug capabilities enable simpler system maintenance/repair

BLOCK DIAGRAM OF PARALLEL PROCESSOR SYSTEM DESIGN UTILIZING OPTICAL "CONCENTRATORS" AND HIGH SPEED OPTICAL COMMUNICATION CHANNELS



Fiber Optic System Interconnect
 $32 \times 32 \times 160 \text{ Gbps} = 164 \text{ Tbps BSSBW}$

Optical "Concentrator" Components

2.5 Gbps electrical signals from
 ASICs X 64 channels = 160 Gbps
 10 Gbps optical channels X 4 color WDM X
 4 Fiber Cable = 160 Gbps

Legend

- Intra-Board Optical Concentrator
- Intra-Board Optic Cable
- Inter-Board Optical Concentrator
- Inter-Board Optic Cable

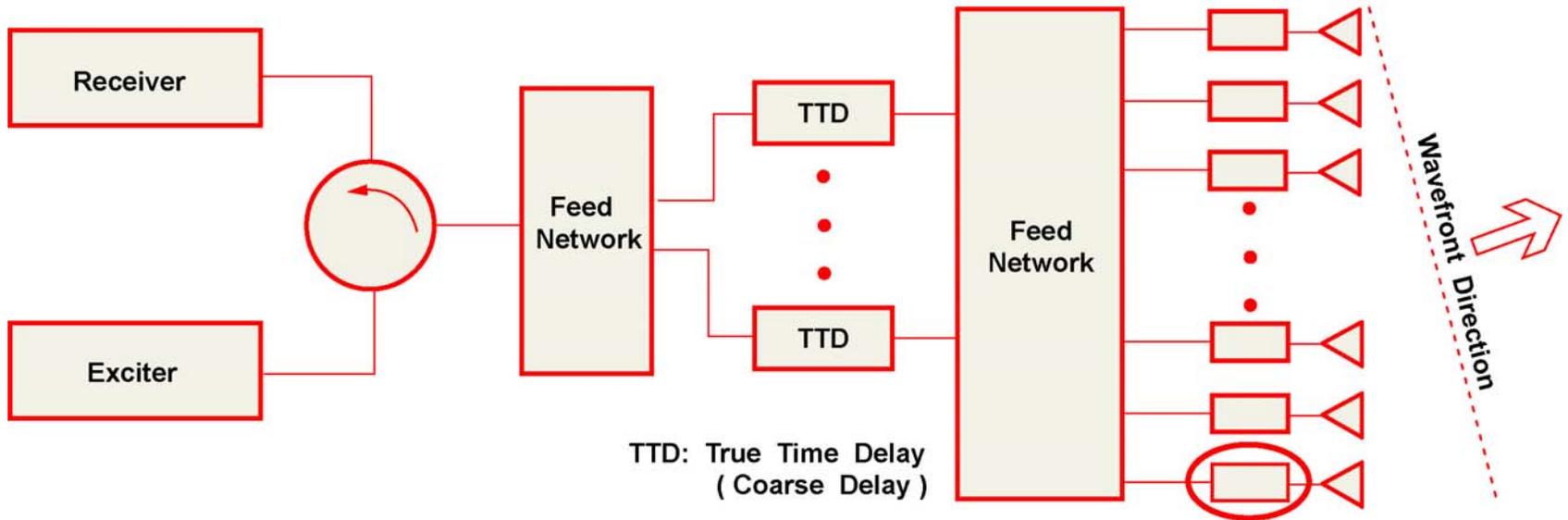
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SYSTEM NEEDS FOR C2OI

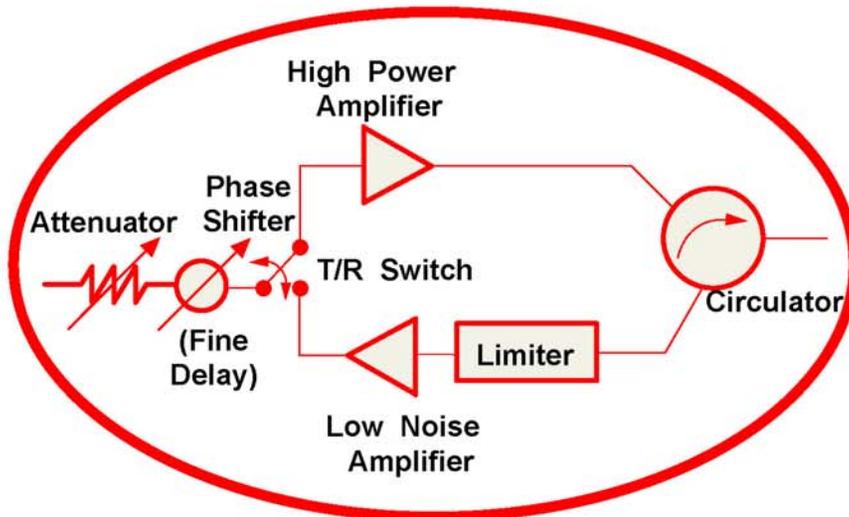
- High End Compute Systems-Freightliner Parallel Processor
- Phased Array Antennas-Active Electronically Scanned Arrays (AESAs)
- Other?

CONVENTIONAL ARCHITECTURE FOR ACTIVE ELECTRONICALLY SCANNED ANTENNA (AESA) (Analog Beamforming)

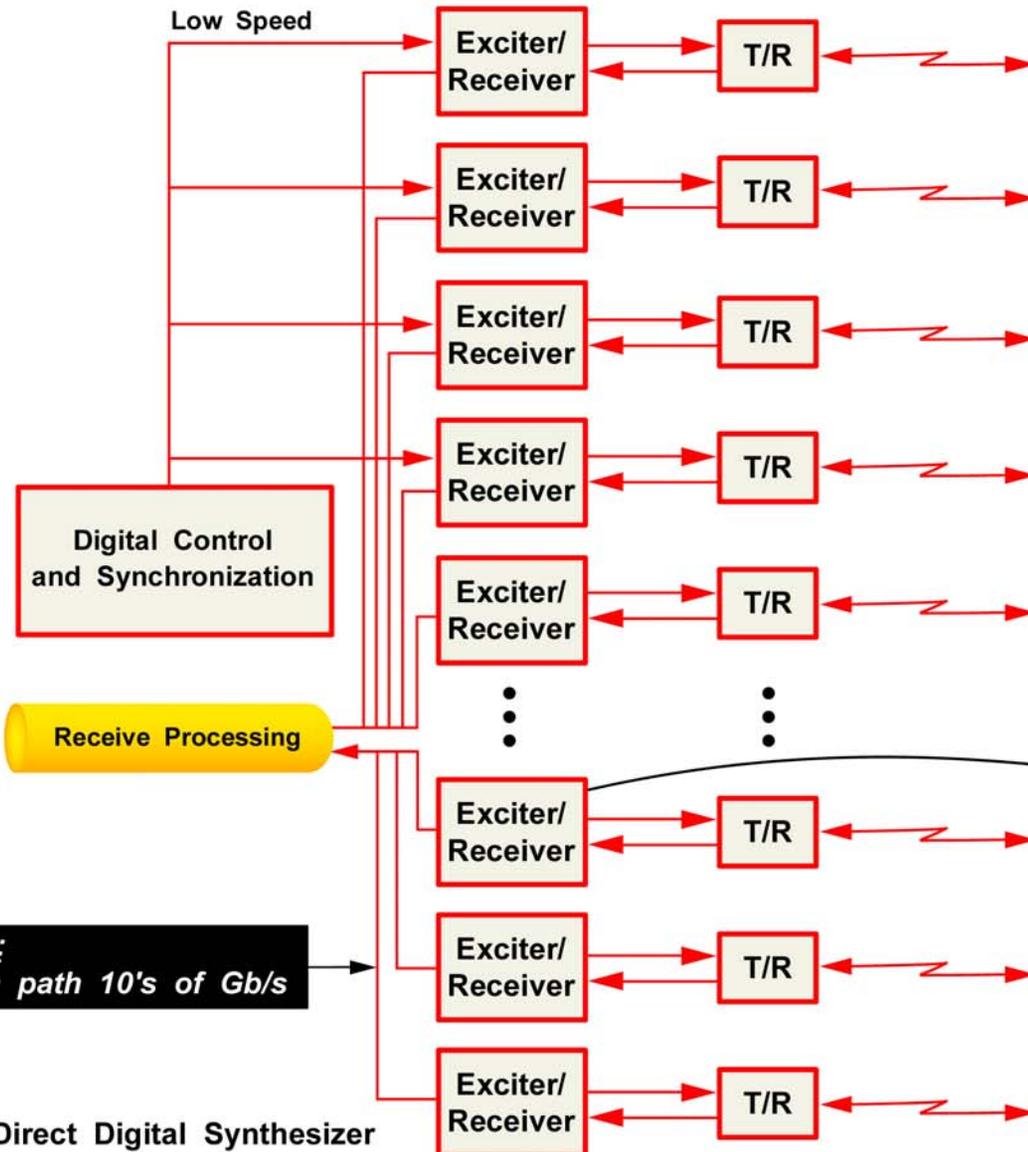


TTD: True Time Delay
(Coarse Delay)

TRANSMIT / RECEIVE (T/R) Module



FUTURISTIC ACTIVE ELECTRONICALLY SCANNED ARRAY (AESA) ARCHITECTURE (Digital Beamforming)

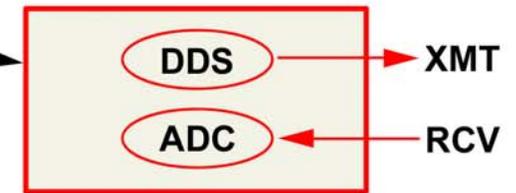


Advantages:

- Fine Control Over Each Element - Multiple Beam Agility
- No Mixers
- No Analog Time Delays
- Wide-Bandwidth Friendly

Problems / Bottlenecks:

- Receiver / Exciter Power
- Tb/s Digital Data Transmission
- Tb/s Digital Data Processing / Storage



Key Elements

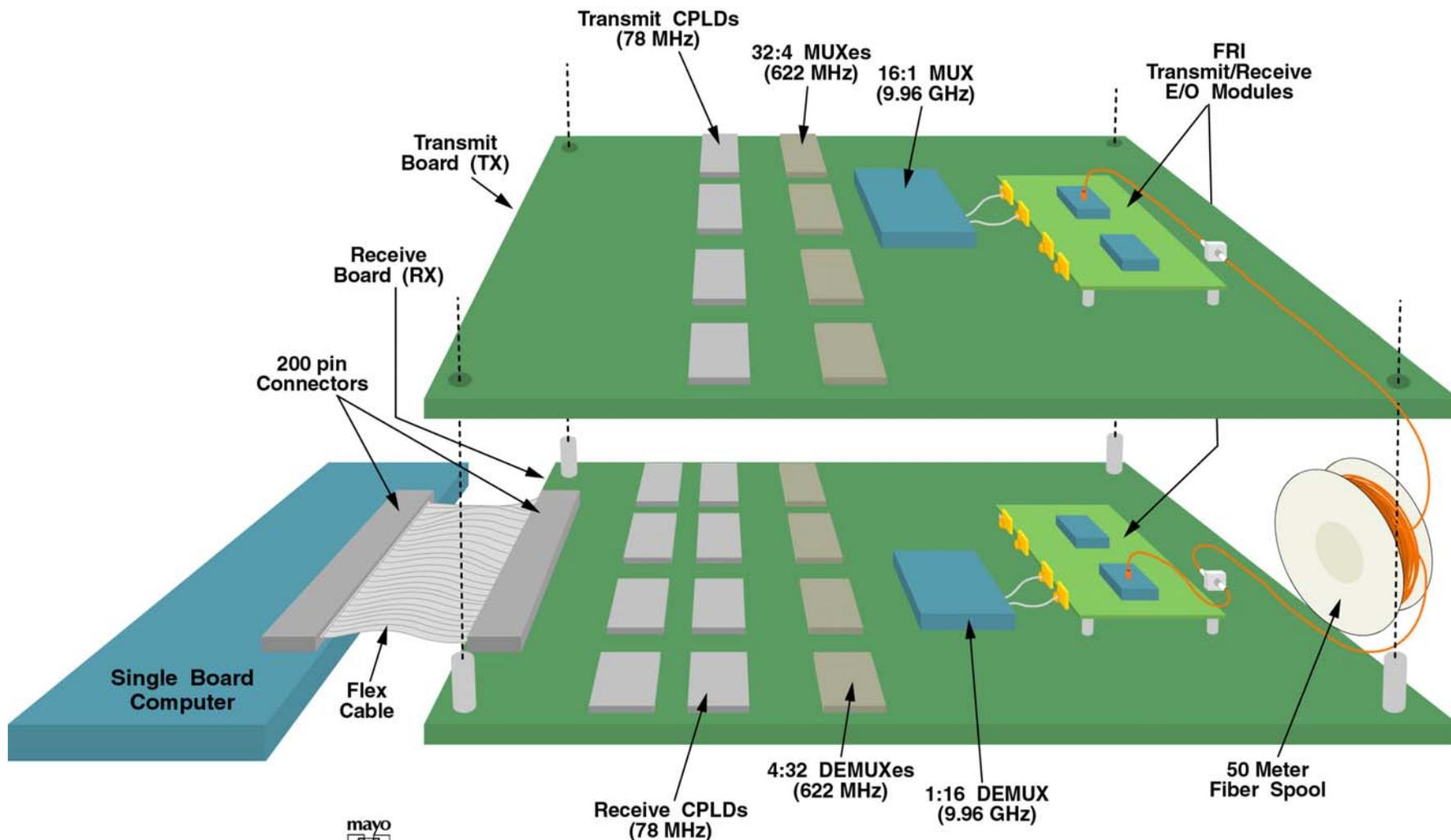
SYSTEM TO DEMONSTRATE 10 GIGABIT/SEC (OC-192) VCSEL-BASED FIBER OPTICAL LINK TARGETED FOR TEST FLIGHTS AT CHINA LAKE NAVAL AIR WARFARE CENTER

(CPLD Components for Bit Error Rate Detection

Provided by China Lake; Board Design Provided by Mayo;

Electrical/Optical (E/O) Transmit/Receive Module Provided by Focused Research, Inc.;

Multiplexers (MUXes) and Demultiplexers (DEMUXes) Purchased from GIGA)



MAYO'S ROLE IN THE C2OI PROGRAM

- Study potential system applications for C2OI
- Provide system application guidance to core C2OI technology team to other government based systems
- Support the testbed application development efforts planned for phases 2 and 3
- Other?

MAYO C2OI PROGRAM PLAN

- Team completes final draft plan of C2OI program
- Evaluate multiple system application opportunities:
 - Government parallel processor system
 - Government AESA applications
 - Commercial large-scale compute systems
 - Others?
- Review, evaluate recommend and ratify system application with the C2OI team
- Schedule to be released

SUMMARY

- Mayo SPPDG can provide a broad array of high frequency technology design, development and characterization capabilities
- Mayo's role for the C2OI program is to provide intra-program applications perspective from a non-competitive professional position
- We see an urgent need emerging from multiple applications for the technology under development in the C2OI program
- Please feel free to contact Mayo at any time at:

Jim Kruchowski

507-538-5469

Kruchowski.james@mayo.edu

- Once the C2OI program is established and under way, we will be contacting each of you for your inputs

MAYO COLLABORATION ON THE CHIP-TO-CHIP OPTICAL INTERCONNECT (C2OI) PROGRAM

OBJECTIVE:

- **Demonstration of Maximum Optical Communication Data Rates and Channel Densities in an Integrated System Packaging Environment**
- **Identify a System Application Where the C2OI Program Development Objectives Can Make a Significant Impact on Overall System Performance**
- **Demonstrate the Finished Component(s) in a System Testbed Applications Environment**

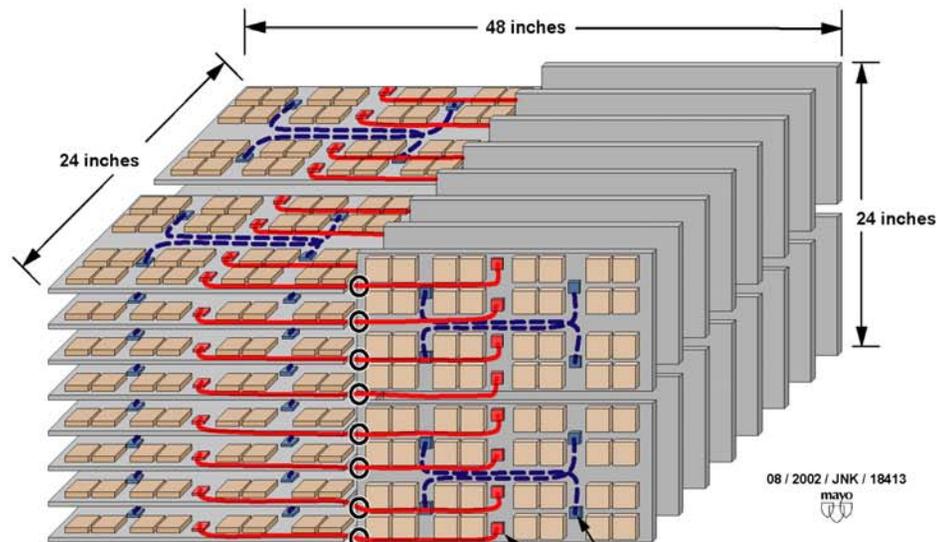
KEY PLAN MILESTONES:

- **C2OI Program Schedule Defined**
- **Define Primary Objectives for System Testbed**
- **Evaluate Potential System Applications**
- **Review and Summarize Testbed Applications with C2OI Team**
- **Select Final Application and Proceed with Phase 2 and Phase 3 Programs**

STATUS:

- **Mayo SPPDG Currently has Several System Development Relationships Under Way that may be Appropriate Systems for this Program**
- **Program Start**

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Legend

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