

Thank you Elias, Good morning. I'm Christie Marrian and I am in the midst of a stint at DARPA's MTO, being officially 'on detail' from the Naval Research Laboratory in Washington DC.

As you may have gathered by now, I was not raised around here. In fact, I joined the NRL some 20 years ago following an education on the other side of the "Pond" that separates the New World from the Old.

DARPA is certainly an interesting place to work. Many other adjectives spring to mind but dull is definitely not one of them.

I'd like to thank Bob, Xan and Frank for giving me this opportunity, although the main blame slash credit must go to Fabian Pease (my predecessor at DARPA) and his then boss Noel Macdonald.

Today, I'd like to provide a perspective on some of the work being pursued in DARPA's MTO under the general classification of "Electronics". The theme of my presentation will be that of the size of electronic devices, and the consequences, mostly extremely exciting, of continued device downscaling. A more materials centric perspective on Electronics will be given by my colleague Edgar Martinez, later this morning.

I should also like to thank my colleagues Jim Murphy, Dave Patterson and Dan Radack who along with Edgar have helped me put this presentation together.

Here we see my version of the famous Moore's law which I've chosen to present in terms of minimum feature size on integrated circuits in volume production.

The plot traces the evolution of this feature size from the invention of the "integrated circuit," to today where we have reached around 150 nanometers.

Incredibly, the minimum feature size on integrated circuits has halved every 3 years. This phenomenon, driven by economic considerations, has resulted in the remarkable increase in information processing that we have on our desktops and in our briefcases.

In fact, I wrote these words on a laptop, that would have been classified as a supercomputer only a dozen years ago. And I wrote most of them at the back of an aircraft in a seat whose dimensions seem to have undergone a similar downsizing.

However, is there an end in sight? (To downsizing transistors that is not aircraft seats) Maybe, but my view is that the end is still a long way off, beyond my retirement age for certain.

At the bottom of the chart, I have included the size of molecules that are being designed to have the same functionality as today's transistors. I will describe some such devices in more detail in a minute.

But first, let's review the prospects for continued downscaling of more conventional solid-state transistors into the nanometer regime.

Here we see, what was, last year at least, the world's smallest transistor. Developed at UC Berkeley under DARPA sponsorship, it shows we can downscale variations on today's transistors to much smaller dimensions than had been thought.

However, some changes in transistor design are going to be needed. For example, here the current flows in a plane perpendicular to the surface of the underlying wafer as opposed to 'in' the plane of the wafer which is the case for conventional transistors.

It turns out that this is a key design change as it permits continued transistor downscaling.

I should stress that these devices have actually been built and they have respectable drive characteristics.

The UC team, along with others in the DARPA program, do not believe this represents the limit to downscaling and a further reduction of over a factor of two is possible.

However, perhaps a greater challenge remains at the circuit architecture level. Assuming, of course, that the admittedly not inconsiderable problems of chip-scale integration will be overcome.

To put it bluntly, what on earth are we going to do with hundreds of billions of transistors in a single chip?

This is a challenge that is occupying our thoughts at DARPA at present, and we are looking for creative ideas. In particular, how large a circuit do we have to build to demonstrate that we are on the right track towards the effective use of these billions and billions of transistors.

I should add that the hardware folks haven't exactly run out of ideas either. For example, they are investigating ways of stacking layers of transistors in 3D which will increase the number of transistors in a chip even more!!

I'll return to this issue but first I'd like to make a small, but very important, diversion, to consider the challenges inherent in the fabrication of these integrated circuits.

Patterning is a key issue, particularly for small volume production which is often needed for DoD specific applications. Advances in projection lithographies have come at a considerable cost: the cost of the mask itself. This does not yet look prohibitive for large production runs. But a run of, say less than 1000 wafers, will become prohibitively expensive if projections of mask costs prove to be correct.

So if the mask is the problem, can we eliminate it, and pattern without masks?

The slide illustrates an approach currently being investigated by ETEC with help from DARPA. The key point to note from this is, that whatever technique will be used in a maskless lithography system, it will require parallelization of the writing technology.

For example, the ETEC approach is to use arrays of miniaturized electron beam columns, each of which occupies a footprint of about two square centimeters. Interestingly enough, miniaturization does have some benefits. Here, for example, the detrimental effects of electron scattering are significantly reduced through use of the miniaturized columns.

We are also interested in more radical alternatives to projection lithographies.

This process, pioneered by Steve Chou at Princeton, is based on a technology for making compact disks. A rigid mold is pressed into a film of a viscous fluid which is then allowed to set by, for example, cooling below its glass transition temperature. The mold is then separated from substrate leaving the pattern imprinted in the solidified film.

Astonishingly enough, this process works a lot better than you might think!

For example, by applying a thin film of a Teflon type material to the mold, separation of the mold can occur without tearing the patterned layer from the substrate.

Defects are the traditional objection raised against contact printing of which this is an innovative variation. However, our colleagues at the University of Texas have observed that the same layer used to aid mold separation results in self-cleaning of the mold.

Thus, as a series of nanoimprints is made, the defect level in the printed patterns improves with each successive print!

This almost seems like magic to me, but I am an electrical engineer by training, so what do I know!!

But seriously, I believe that this ability to understand and tailor surface properties with the appropriate chemistry is key.

Indeed, it is the breakthrough that makes contact printing worth pursuing again after it was abandoned some twenty-five years ago.

This may seem radical but don't forget, an awful lot of compact discs are fabricated with similar techniques for around 1\$ a disk!!

Still, we are not there yet. We are currently concerned with the issue of multilevel alignment as well as putting the defect issue well and truly to bed.

Oh, I nearly forgot to mention that the resolution of these printing techniques is phenomenal.

Replication of 3 nanometer features has been demonstrated which means this technology has a resolution about 50x better than today's production lithographies!

But enough lithography, let's return to electronics and device technologies.

So the prospects for reaching the nanoelectronics regime based on extensions of existing technology look promising. But DARPA is also looking beyond this.

As I mentioned when introducing downscaling, molecular based electronics offer the promise of electronic devices with even smaller sizes.

We are also looking for some help with the fabrication challenges by taking the molecular route. The idea is that we can design the molecular switches so that they will assemble into circuits rather than having to be placed individually.

So to paraphrase the 50's slogan "Better living by Chemistry", we are hoping for "Cheaper fabrication through Chemistry" (and perhaps Biology ... but that is another story!) However, a consequence of using energy driven assembly is that there will almost certainly be defective components in our molecular circuits.

We have to learn how to cope with these defects. This adds new constraints on the architecture of future molecular electronics systems.

A key element will be the way in which the individual components are connected together. For example, interconnection schemes must allow reconfiguration so the molecular circuit can operate even when a significant number of the components are defective.

And as I mentioned earlier, these new architectures must be scalable.

That is they must remain valid as we reach integration levels of 10^{12} devices.

So, how far have we come in our quest for molecular based electronics?

We are used to designing and synthesizing organic molecules to have a desired chemical or material property. Now, we are getting the hang of designing molecules with a desired electronic functionality.

Here is an example. This molecule has two conduction states that can be switched electrically by applying a voltage across the molecule. This results in this highly non-linear "I-V" characteristic which is, in many ways, reminiscent of a resonant tunneling diode.

In fact, as an electrical engineer, I would like very much to be able to design a resonant tunneling diode with this good a characteristic! This molecule was synthesized by Jim Tour at Rice and integrated into a nanopore memory by Mark Reed at Yale. Mark assures us that the memory has operated at room temperature far longer than the attention span of his most conscientious graduate students!

A different approach to molecular memory is being pursued at Harvard. This is a simple switch based on two crossed carbon nanotubes. The memory is actually reminiscent of a relay as its actuation is electro-

mechanical in nature. A potential, applied between the nanotubes, causes them to snap together forming a low resistance junction.

Simply applying the reverse potential causes the nanotubes to separate. Note there is a difference of 5 orders of magnitude in the resistance of the two states. Because it is so incredibly small, this "relay" can be operated at very high frequencies.

A further advantage of molecular based electronics is that we can now think of alternative manufacturing technologies. The aim is to assemble, rather than fabricate, molecular based circuits. By assemble, I mean that a circuit will be formed spontaneously by processes which are driven by energy minimization.

Here are some examples.

We can arrange for molecules, here carbon nanotubes, to grow at predefined locations through appropriate catalysis design. I should add the Oak Ridge team clearly recognize the importance of acknowledging their sponsor.

Our colleagues at Penn State use electrostatic energy minimization to position metallic nanowires with nanometer precision.

Shown at the bottom left are 3 nanowires chained end to end.

Lastly, the team at HRL use fluidic assembly to position larger objects. Here, 200 micron glass spheres have been assembled into the positions defined by the array of squares. In this case, surface energy minimization is the driver.

Note how each of these examples represents a different type of energy minimization and that each process has been designed to operate at different length scales.

DARPA's Moletronics (as we call Molecular Electronics) is run jointly by MTO and the Defense Sciences Office. On Friday morning, you will hear a more 'animated' presentation about this exciting program from my partner in crime, Bill Warren from DSO.

In spite of the promise shown by molecular based electronics, there will always remain applications where the preferred approach is to develop new semiconductor materials.

Extremely high-speed devices are an example.

We have come a long way in creating 'designer' compound semiconductors with the physical properties that enable increased system performance. Recent advances in materials growth technology have realized the Antimonide family of semiconductors. These materials promise us the extremely high-speed electronics at the low consumed power vital for tomorrow's autonomous vehicle based applications.

Also, because of the unique band gap arrangements (shown in the inset), these materials point the way to the development of powerful new infrared sources and detectors.

Another great challenge in nanoelectronics is illustrated in this proposed approach to scalable quantum computing. The challenge is to fabricate a large number of essentially atomically identical Nano pillars each with a carefully designed stack of thin layers of material.

Maintaining the identical electronic properties of each Nano pillar in the array is going to be extremely difficult.

But this scheme does at least circumvent another of the great nanoelectronics problems. Namely, how does one interconnect nanoelectronics devices?

In this case, interconnect wiring is not required as the nano pillars are to be addressed with photons.

Again this points out that as we move into the nanoelectronics regime, we need to consider new system architectures rather than just new device concepts.

So I hope I have given you a flavor of where we see the exciting opportunities as microelectronics reinvents itself as nanoelectronics.

We believe that electronics remains key to Microsystems Technology. And that breakthroughs in the field will continue to have revolutionary implications for Microsystems Technology as a whole. I look forward to discussing these issues with you at the posters and sidebars.

In closing, I'd just like to thank you for your attention and put in a plug to join with us at DARPA.

The job is, above all, not dull and where else can you get to use a teleprompter and be shown on these huge screens without becoming a politician, rock star or media talking head!!